EXPERIMENTAL 20 GBIT/S MODULES FOR OPTICAL FIBER LINKS

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ABSTRACT

For an experimental optical fiber transmission system working at 20 Gbit/s electronic transmitter and receiver modules were developed. To guarantee reliable and error free operation, unpackaged GaAs- and Si-chips on ceramic thinfilm substrates in combination with a sophisticated interconnection technic had to be used.

INTRODUCTION

There has been a fairly steady trend toward employing high and ultra-high bit rates in optical transmission systems for more than ten years now. The fact that current optical transmission systems, at least experimental types, are capable of handling bit rates of several 10 Gbit/s largely due to marked advances in the field of monolithic silicon and GaAs digital integrated circuits [1]. The prerequisites for generating and processing high-bit-rate optical signals are employing suitable types of circuit architectures and fabrication technologies, circuit designs based on microwave technology, and the availability of fast semiconductor circuit components.

EXPERIMENTAL OPTICAL 20 GBIT/S SYSTEM

For an experimental optical system the schematic circuit diagram is given in Fig. 1. Two data signals of 10 Gbit/s each, e.g. two STM-64-signals, are multiplexed synchronously in the transmitter module into one 20 Gbit/s output signal which after amplification by a driver circuit controls the optical modulator. For transmission experiments over fiber links and for measurements of optical and electrical components the use of pseudo random sequences with maximum length is advantageous. In our system we use two generators which are synchronized in such a way, that the output signal of the slave is delayed by half the wordlength with respect to the master. In this case, after multiplexing these signals bit by bit, a sequence of maximum length can be obtained again. Each of the generators is realized by only one monolithic integrated Si-chip. The word lengths of their output patterns can be switched between $(2^{15}-1)$bit and $(2^{23}-1)$bit.

The laser light is modulated by the 20 Gbit/s-signal in NRZ-format. At the end of the fiber link the optical signal is reconverted into the original two 10 Gbit/s data streams. After detection of the light signal in a PIN photo diode the electrical 20 Gbit/s signal is amplified in a transimpedance amplifier followed by a preamplifier to get sufficient amplitude for controlling the signal splitter. This circuit is a resistive 6dB coupler, because a preamplifier with differential outputs is still under development as well as the decision circuit. Both will be monolithic integrated Si/Ge circuits. The demultiplexer splits the regenerated bit stream into two 10 Gbit/s signals, which can be used for error rate measurements or SDH signal processing.

TRANSMITTER MODULE

The transmitter module consists of six GaAs-chips which are mounted on a ceramic thinfilm MIC. It has the size of 2 by 2 square inches. The GaAs-chips are of NLG 4000 (MUX, decision circuits and clock distributor) and CI 4600 (DFF and frequency divider) families from NEL. The 20 GHz power divider is a 3dB/180° ring coupler in microstrip line technic and has not been included to the module till now. This gives us the possibility of phase tuning of the DFF clock signal to obtain optimal eye-diagrams of the 20 Gbit/s output signal. The output amplitude of the module is 1 V_{PP}, therefore an additional modulator driver is necessary for this purpose to reach 6 V_{PP}.

The decision circuits as input stages are used to be more independent of input signal amplitude and level. For that reason we even can process signals from some special Si-circuits which only reach 200 mV_{PP}. As an additional advantage the input signals are clocked before feeding them to the data selecter. The data selecter works as a 2:1 bit-multiplexer, its output is switched between the two input signals by means of a 10 GHz clock signal. The adjacing DFF is clocked by 20 GHz and optimizes the eye diagram of the 20 Gbit/s output signal with respect to jitter, symmetry and eye opening.

RECEIVER MODULE

At the receiving end, Fig. 3, one needs a conventional TDM-receiver with clock recovery circuit, regenerator for both, amplitude and phase, and demultiplexer 1:2. The receiver module has also the size of 2 by 2 square inches; the DFFs, the clock distributor, the Exclusive-OR gate, and the frequency divider are GaAs-chips.

Since the 20 Gbit/s decision circuit is still under development, in the mean time we use a 20 GHz D-flipflop as

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amplitude and phase regenerator. The 2:1-demultiplexer consists of two 20 GHz D-flipflops, too. They are clocked by two 180^0 phase shifted signals which can be changed by means of a channel synchronizing signal (Synch in) to get the same channel coordination as at the transmitting end. As already described for the transmitter module the 20 GHz clock inputs are fed separately to the module to be able to match the clock phases of input stage and demultiplexer flipflops independently of each other.

CLOCK RECOVERY CIRCUIT

The passive clock recovery circuit is a monolithic integrated GaAs circuit, too. It was developed at Fraunhofer Institut, Freiburg, Germany, in connection with a research contract. The circuit consists of preprocessor, a full-balanced narrowband regenerative frequency divider loop, a phase shifting and a limiting amplifier. It can be operated at 10 and 20 Gbit/s [2,3].

ASSEMBLING TECHNIC

For the 20 Gbit/s modules we developed a new possibility of inserting and inner lead bonding of semiconductor chips in film circuits [4]. This technology, which we call "Reverse Beam-Lead Interconnection Technology", is suited, apart from its generally favourable applicability to the setup of multi chip modules, especially for the implementation of ultra high-speed circuits. The basic principle of the chip interconnection technology presented is that the semiconductor chips to be inserted are mounted flush with the film circuit surface into a previously prepared chip-sized substrate opening from the reverse side of the film circuit. Into the cutoff leads project as part of the film circuit. They are bonded to the chips by means of, for instance, soldering. Adjustment and placement of the chips to the leads are performed individually using a face-down component placement device. The flush chip mounting and the possibility of exact geometrical adaption of the leads to the conducting structure of the semiconductor chips provide a circuit configuration with remarkable low impedance discontinuities and with low electrical attenuation. A description of the photolithographic manufacturing of the lead structure with the contact layers as well as of the bonding process will be given.

Figure 4 shows the front side layout of the transmitter module with all 50 ◈ microstrip lines and with power supply layers for chip capacitors and some termination resistors. These layers are connected with the reverse side by metallized via holes and in case of the ground layers by the partly metallized chip cuttoffs. The ground layer for the micro striplines and all power supply interconnections and hybrid integrated decoupling capacitors are on the reverse side of the substrate. Chip surfaces and substrate surface are on the same level, therefore wire bonds can be made as short and flat as possible. Where 50 ◈ lines cross each other the crossed line is bridged by a 250 µm wide gold ribbon.

Due to thermal problems the distances between the chips are chosen as long as possible because the power dissipation of all chips together is about 9.6 W. The substrate is mounted to a large heat sink which must be cooled by air.

The first four circuits at the left hand side are working at 10 Gbit/s with the exception of the frequency divider. These chips are conventionally wire bonded. The selector and the D-flipflop, however, at the right hand side of the substrate (inside the circle line) are working at 20 Gbit/s. They are connected to the substrate layers by the above discribed reverse beam-lead technic. The extended part in Fig. 4 shows some details. The thinfilm gold-leads, which are connected to the chips by welding are of optimal shape to obtain lowest inductivities for the power supply and ground connections and to guarantee as perfect as possible impedance matching for the 50 ◈ microstrip lines. The advantages of this technic in comparison with bonded wires are remarkable [5]. Nevertheless there are still some points to be improved. The next goal, e.g. is to reduce the gap width between substrate and chip to a minimum, because this gap is responsible for discontinuities of the line impedances and therefore causes reflections. This can be done by precise cutting of chips and substrate cutoffs or by filling the gap with a material with a suitable dielectric constant.

Furthermore we are working on hybrid integrated microwave capacitors basing on polyimid materials. These capacitors shall be used as coupling capacitors as well as bypass capacitors and we try to place them very close to the chips. First experiments with coaxial bypass capacitors inside the via holes show quite satisfactory results.

CONCLUSION

The paper describes two 20 Gbit/s modules for optical transmission experiments as examples for a new chip interconnection technic which is also suitable for microwave applications up to more than 50 GHz. We obtain nearly lossless and non-reflecting interconnections between semiconductor chips and microstrip lines and also ground and power supply interconnections with very low impedances. Each of the modules consists of six unhoused GaAs-chips from NEL (NLG 4000 and CI 4600 families). The thinfilm ceramic substrates are 254 µm thick and have a size of 2 by 2 square inches. They are mounted into microwave packages with K- amd SMA-connectors.

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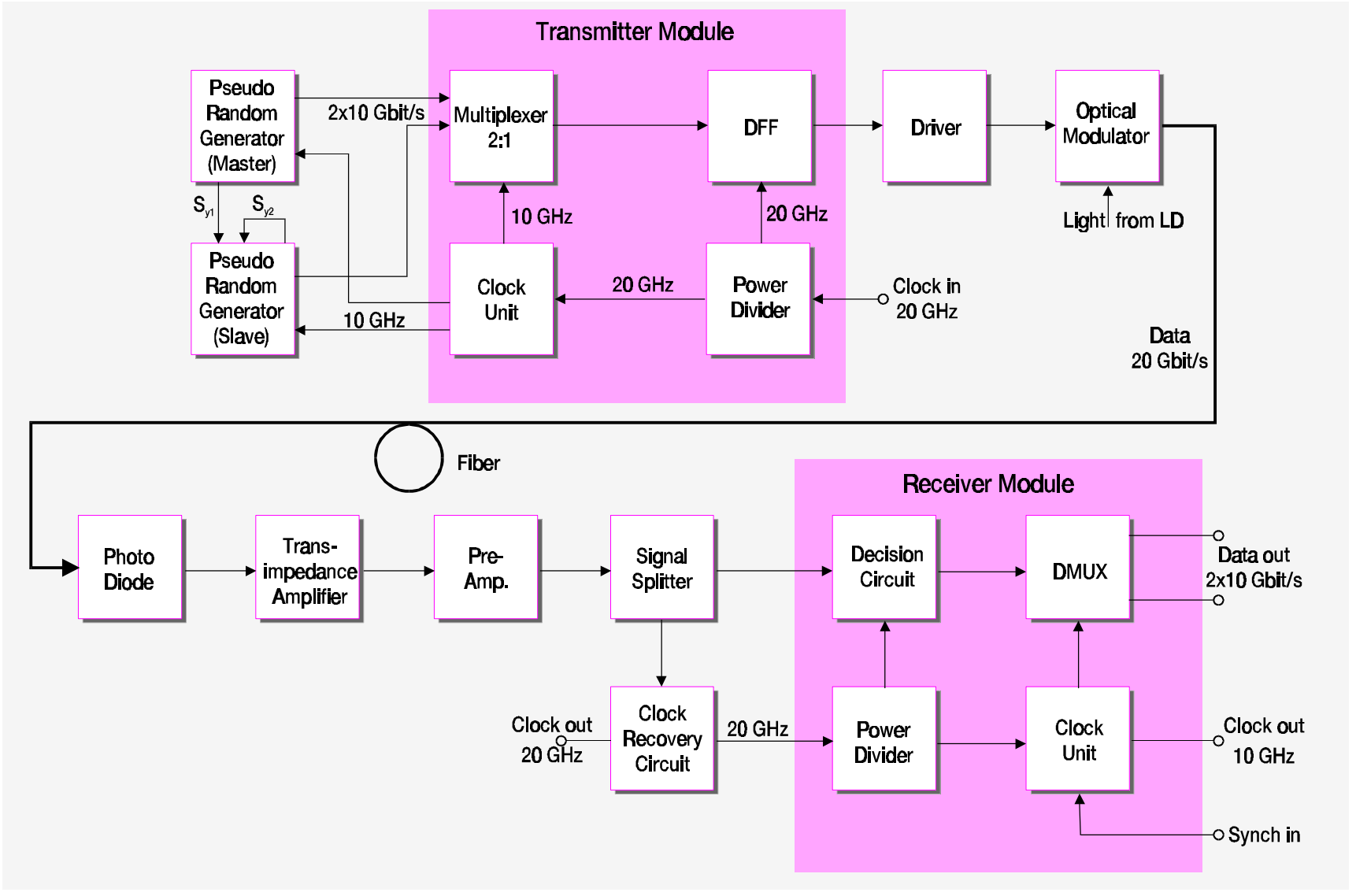

Fig. 1 Schematic diagram of the experimental 20 Gbit/s optical fiber system. Two synchronous 10 Gbit/s signals are multiplexed, transmitted and demultiplexed. The transmitter- and receiver-modules are equipped with GaAs-chips and built up as hybrid thinfilm circuits

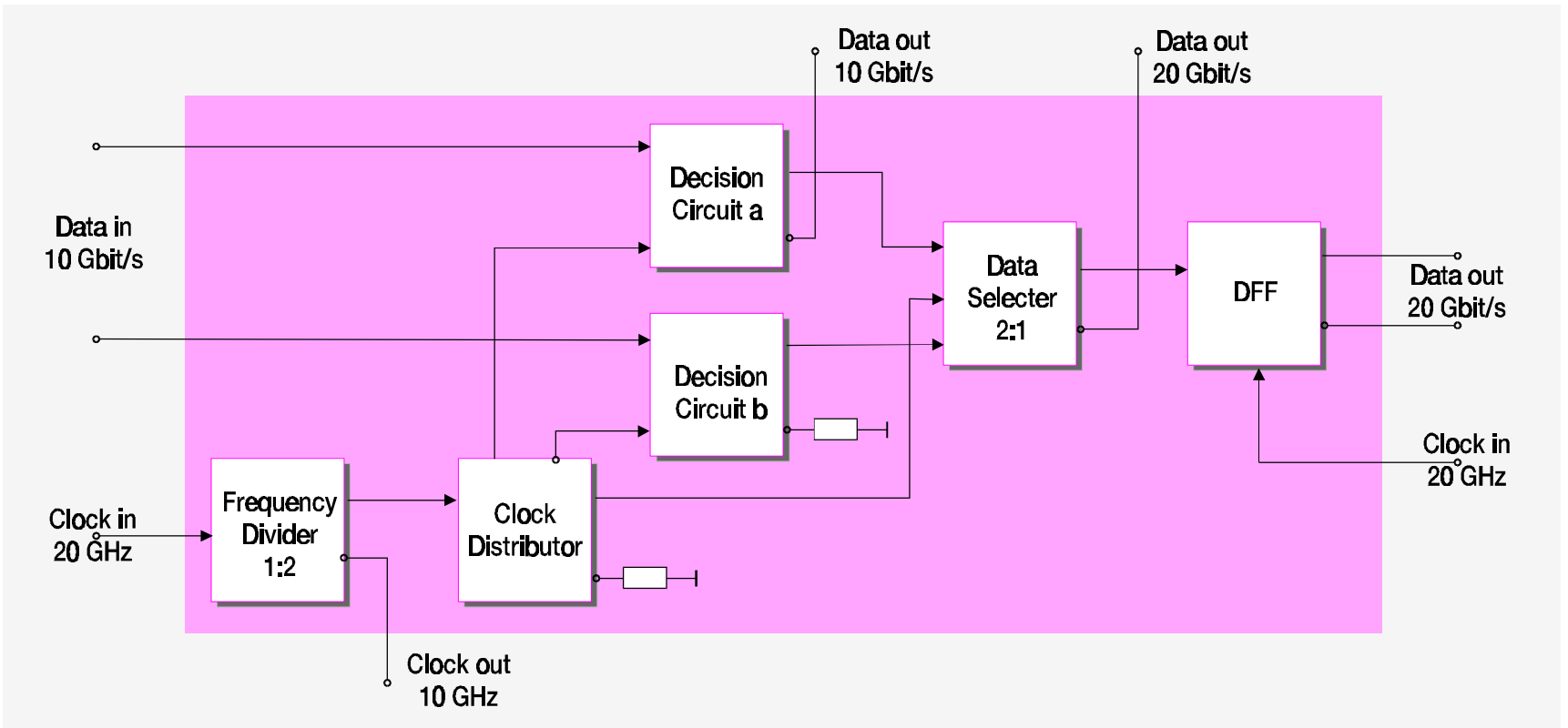

Fig. 2 Hybrid integrated transmitter module in thinfilm-technic, consisting of six GaAs-chips. The two chips at the right hand side, working at 20 Gbit/s, are connected in reverse beam-lead technic, while all other chips are conventionally wire bonded.

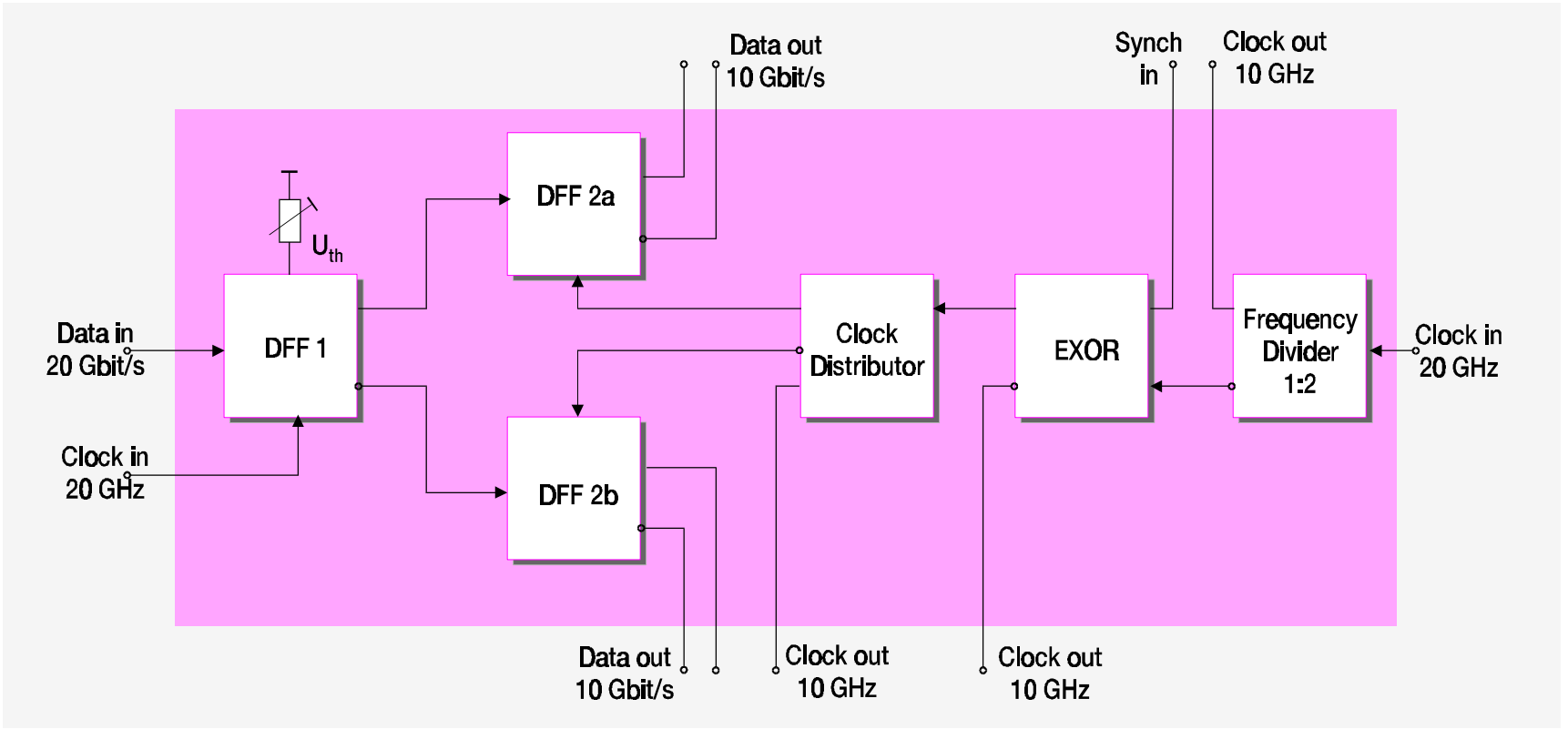

Fig. 3 Hybrid integrated receiver module in thinfilm technic, consisting of six GaAs-chips. Only the D-flipflop at the 20 Gbit/s data input is connected in reverse beam-lead technic, all other chips are wire bonded.

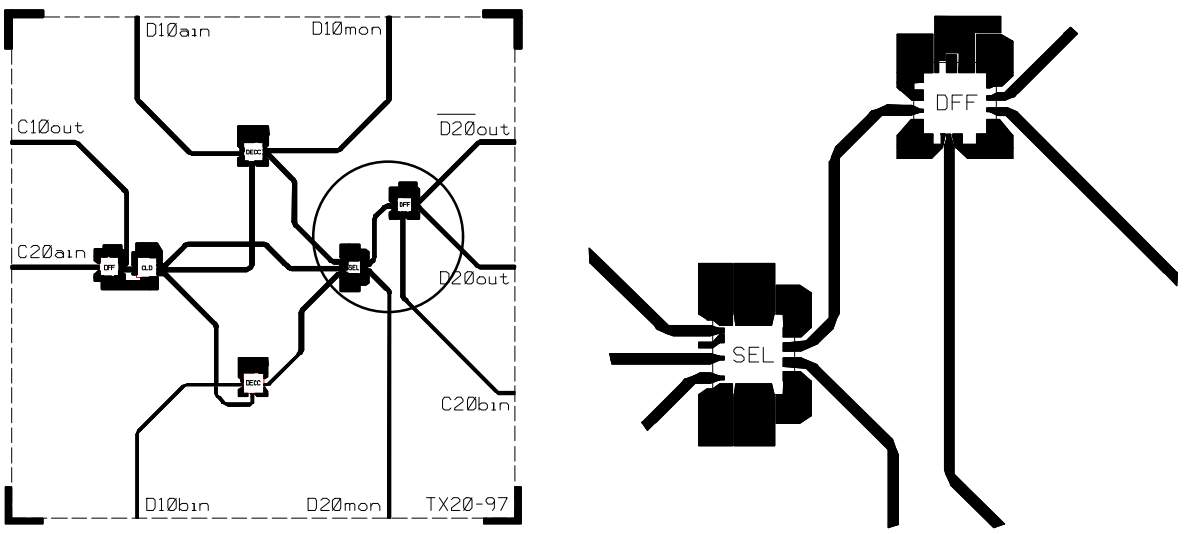

Fig. 4
Layout of the transmitter module. A 254 ✪m thick ceramic substrate has been used for the hybrid integration of the six GaAs chips. The 50 ✧ microstrip lines are 250 ✪m wide, all power supply layers are on the reverse side of the substrate. Only the two circuits inside the circle are operated at 20 Gbit/s and therefore connected in Reverse Beam-Lead technic. Details of their layouts are given at the right hand side.

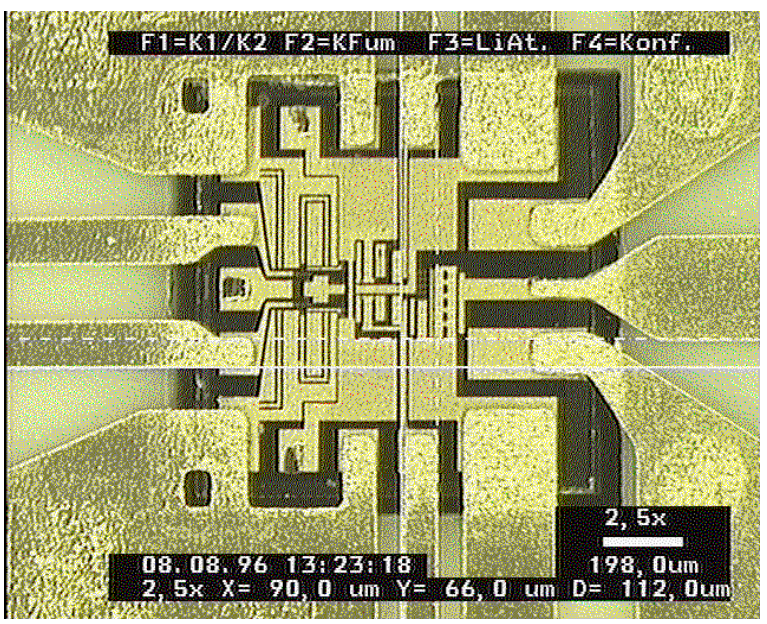

Fig. 5
Example of a GaAs-circuit, connected in "Reverse Beam-Lead Technic". The thinfilm gold-leads are of optimal shape to obtain lowest inductivities for the power supply and ground connections and to guarantee as perfect as possible impedance matching for the 50 ✧ microstrip lines. The next goal is to reduce the gap width between substrate and chip to a minimum or to fill it with a material with a suitable dielectric constant to minimize the reflections.

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